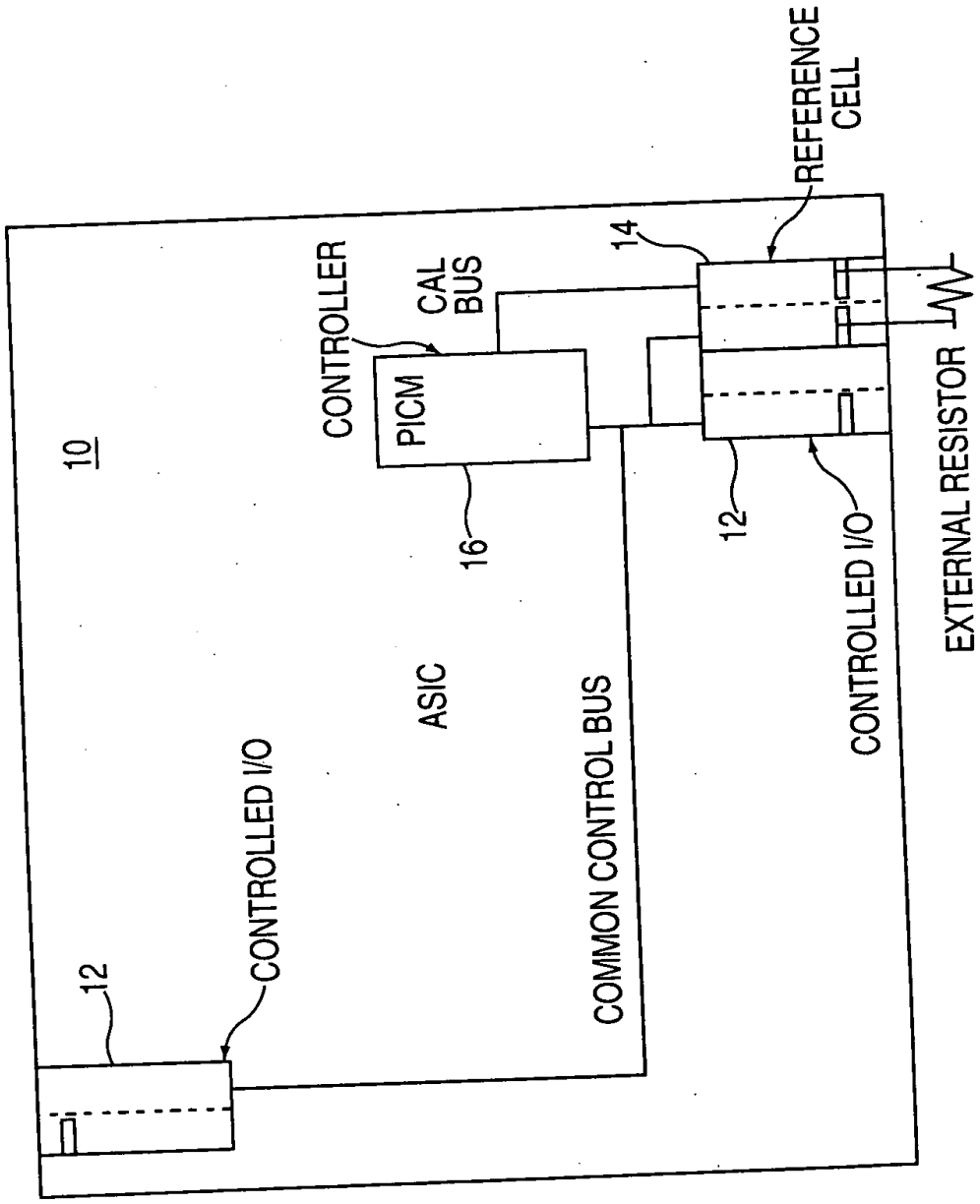


ASIC ARCHITECTURE

FIG. 1

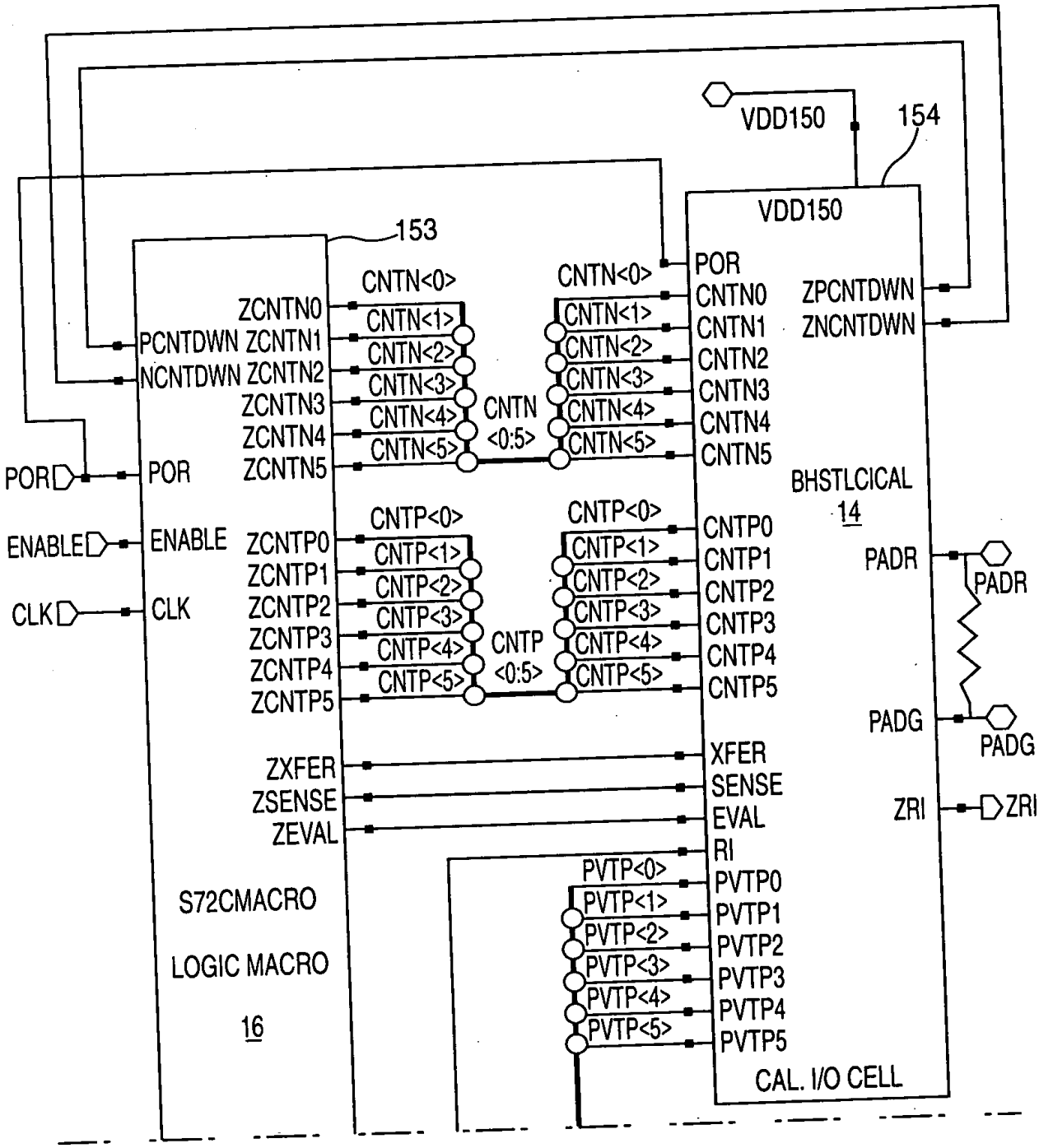


FIG. 2A

2-A
2-B

FIG. 2

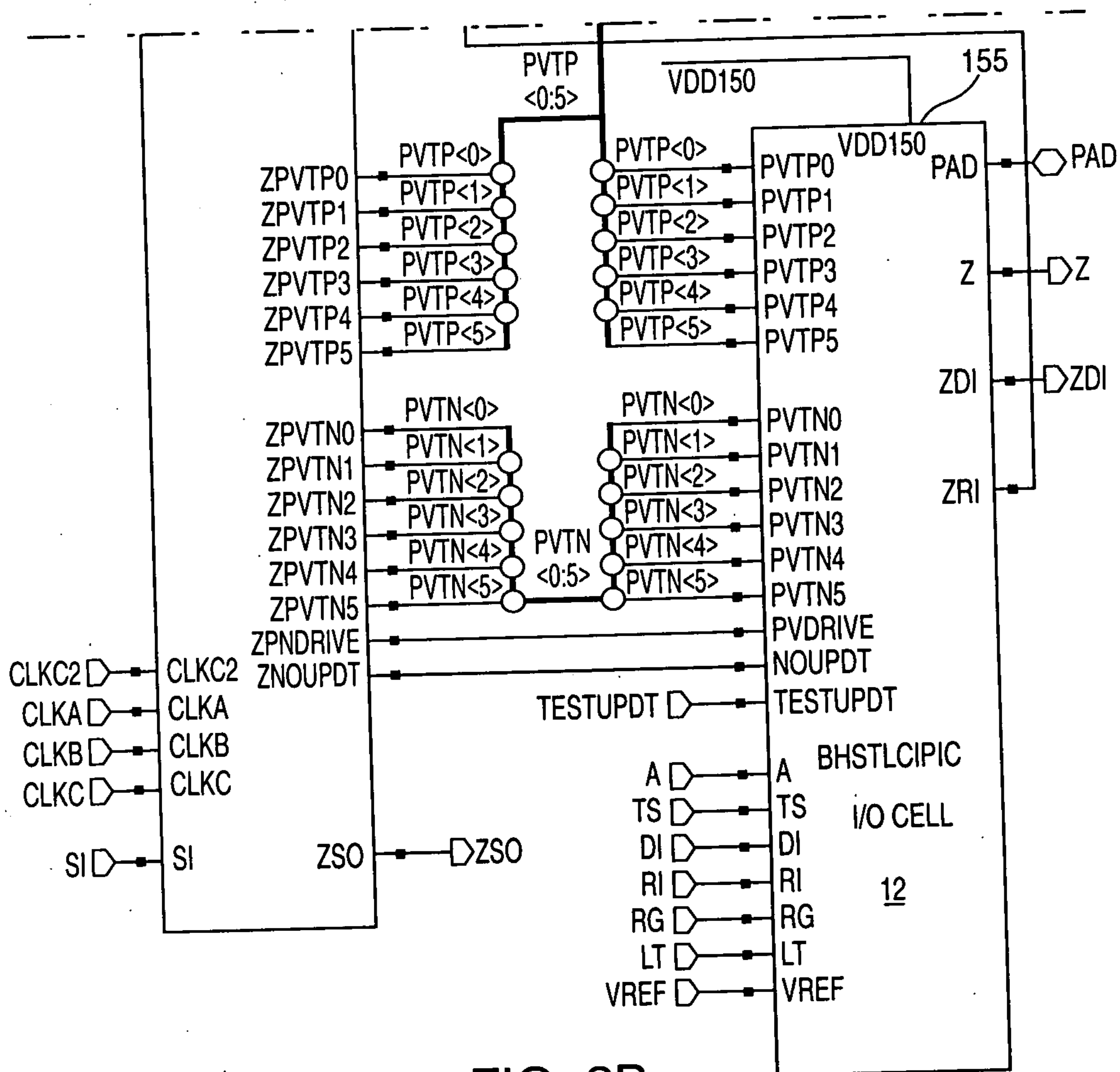
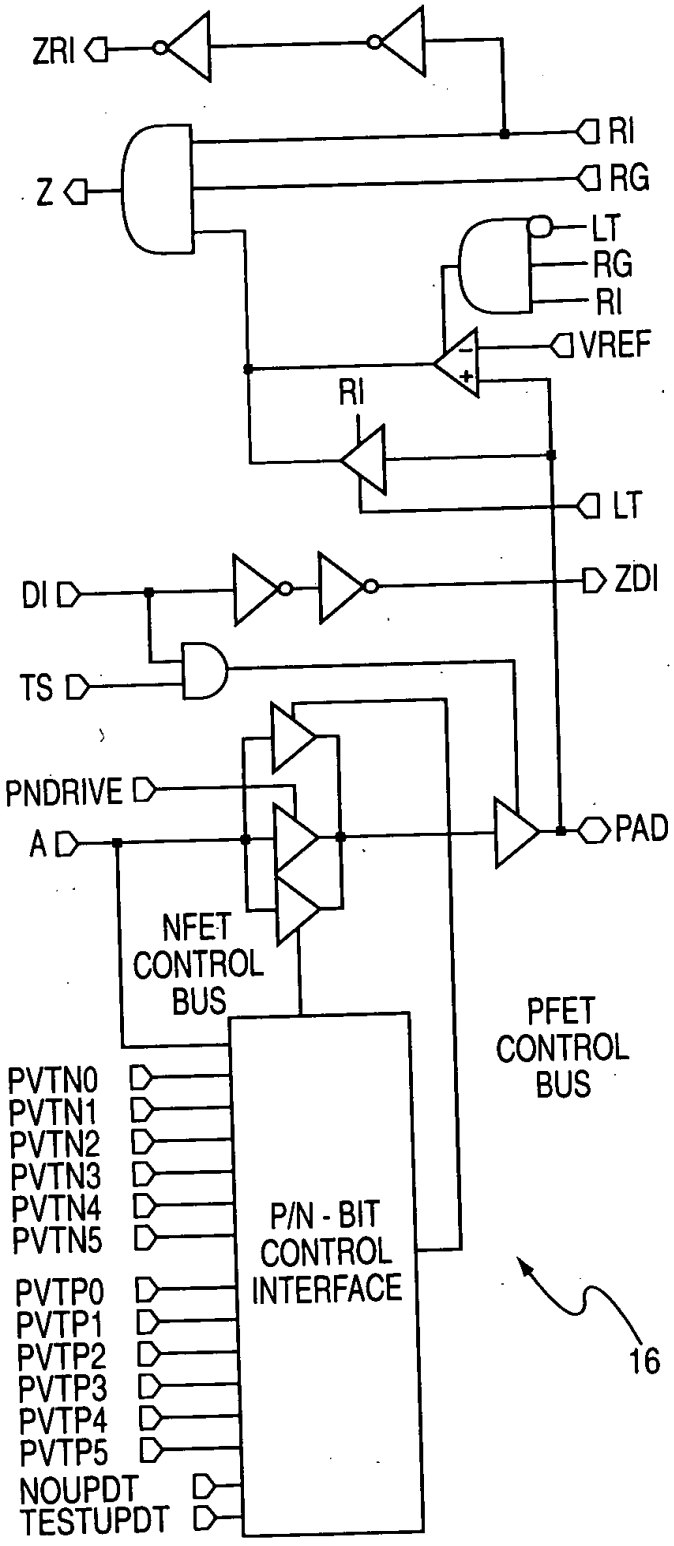


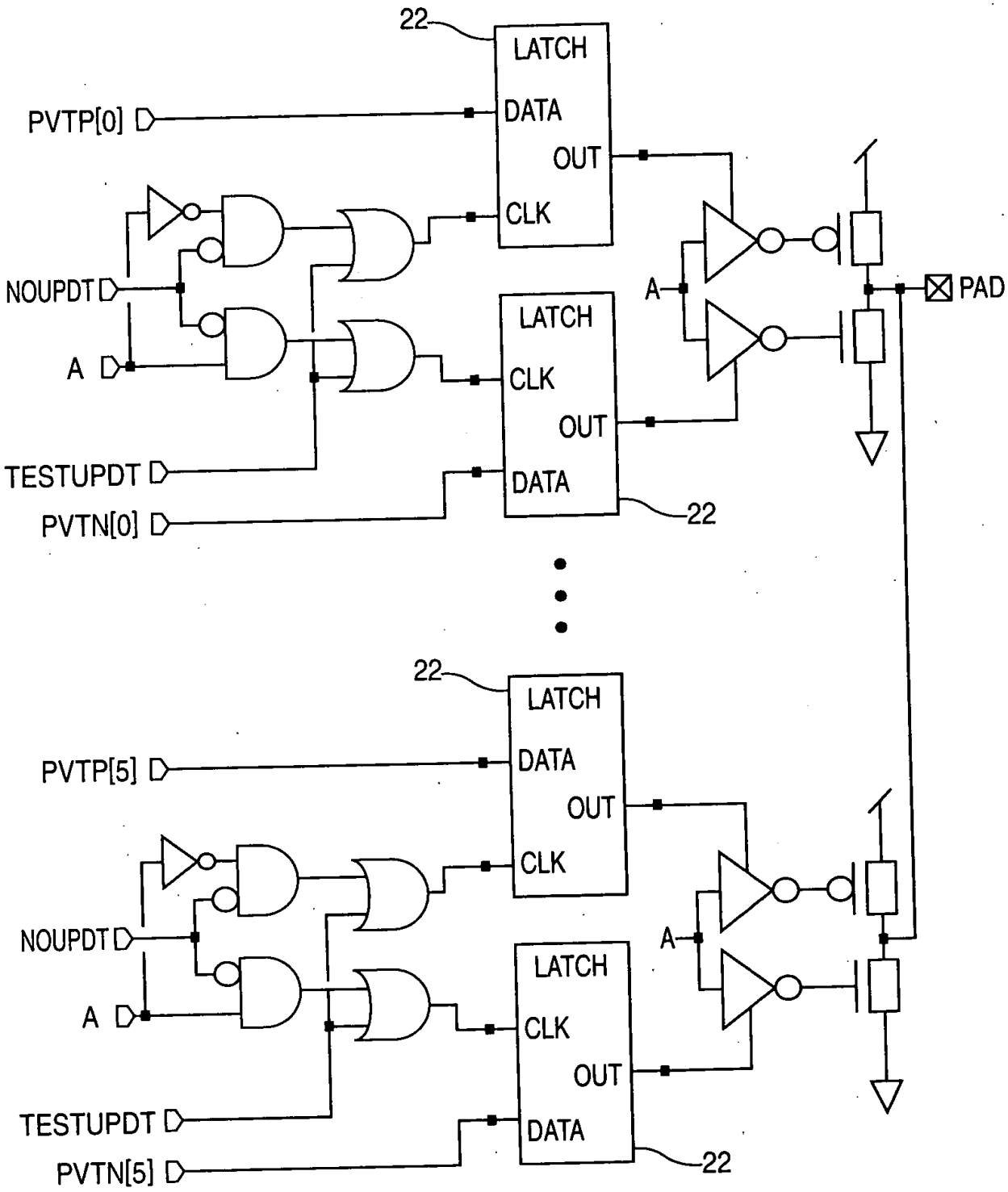
FIG. 2B

A	DRIVER DATA INPUT
TS	DRIVER TRI-STATE CONTROL
DI	DRIVER INHIBIT INPUT (DI IN)
LT	DC CURRENT GATE (I_{dd} TEST) INPUT
RI	RECEIVER INHIBIT INPUT (RI IN)
RG	RECEIVER GATE CONTROL
VREF	VOLTAGE REFERENCE INPUT
PAD	DRIVER OUTPUT/RECEIVER INPUT
ZDI	DRIVER INHIBIT OUTPUT (DI OUT)
ZRI	RECEIVER INHIBIT OUTPUT (RI OUT)
Z	RECEIVER OUTPUT
PVTN0	NFET PVT CONTROL BIT (LSB)
PVTN1	NFET PVT CONTROL BIT
PVTN2	NFET PVT CONTROL BIT
PVTN3	NFET PVT CONTROL BIT
PVTN4	NFET PVT CONTROL BIT
PVTN5	NFET PVT CONTROL BIT (MSB)
PVTP0	PFET PVT CONTROL BIT (LSB)
PVTP1	PFET PVT CONTROL BIT
PVTP2	PFET PVT CONTROL BIT
PVTP3	PFET PVT CONTROL BIT
PVTP4	PFET PVT CONTROL BIT
PVTP5	PFET PVT CONTROL BIT (MSB)
PNDRIVE	DEFAULT CONTROL BIT
NOUPDT	PREVENTS BIT UPDATE
TESTUPDT	UPDATES BITS



CONTROLLED I/O CELL

FIG. 3



DRIVER-IMPEDANCE UPDATE LOGIC

FIG. 4

INPUTS			OUTPUTS		
A	NOUPDT	TESTUPDT	P-BITS	N-BITS	COMMENTS
X	1	0	NC[1]	NC[1]	INPUT BITS CHANGING
0	0	0	UPDATE[2]	HOLD[2]	UPDATE P-BITS ONLY
1	0	0	HOLD[3]	UPDATE[3]	UPDATE N-BITS ONLY
X	X	1	UPDATE[4]	UPDATE[4]	FORCE UPDATE TO ALL P/N-BITS

1. WHEN "NOUPDT" IS HIGH, THE INPUT CONTROL BITS WILL BE UPDATED AND THE I/O WILL HOLD THE PRESENT STATE OF THE CONTROL BITS UNTIL "NOUPDT" GOES LOW. THIS PREVENTS THE I/O FROM CHANGING THE OUTPUT IMPEDANCE WHILE THE INPUT CONTROL BITS ARE UNSTABLE.

2. WHEN THE DATA INPUT "A" CHANGES FROM A HIGH TO A LOW STATE, THE PULL-UP IMPEDANCE WILL BE UPDATED. THE P-BITS WILL BE LATCHED WHEN "A" TOGGLES FROM LOW TO HIGH.

3. WHEN THE DATA INPUT "A" CHANGES FROM A LOW TO A HIGH STATE, THE PULL-DOWN IMPEDANCE WILL BE UPDATED. THE N-BITS WILL BE LATCHED WHEN "A" TOGGLES FROM HIGH TO LOW.

4. WHEN "TESTUPDT" IS HIGH, ALL THE DATA LATCHES WILL BECOME TRANSPARENT AND BOTH THE PULL-UP AND PULL-DOWN IMPEDANCE WILL BE UPDATED.

NOTE: "TESTUPDT" IS USEFUL TO THE USER TO UPDATE THE OUTPUT IMPEDANCE IF THE I/O HAS BEEN SITTING IN Hi-Z OR THE "A" INPUT HAS NOT TOGGLED FOR A LONG PERIOD OF TIME.

DRIVER IMPEDANCE UPDATE TABLE

FIG. 5

INPUTS					OUTPUTS	
A	TS	DI	PNDRIVE	PVTN[0:5] PVTP[0:5]	PAD	ZDI
-	0	-	-	-	Hi-Z[1]	DI
-	-	0	-	-	Hi-Z[1]	D1
-	1	1	0	0	Hi-Z[2]	D1
-	1	1	-	1[3]	A	D1
-	1	1	1	-	A	D1

1. PAD IS Hi-Z IF DRIVER IS NOT EXTERNALLY TERMINATED. PAD IS AT "$V_{ddq}/2$" IF DRIVER IS TERMINATED (OFF-CHIP).
2. PNDRIVE=0 IS FOR TEST ONLY. THIS FORCES THE DEFAULT BIT OFF SUCH THAT THE LSB'S CAN BE TESTED.
3. AT LEAST ONE PVTN BIT AND ONE PVTP BIT MUST BE AT A LOGIC "1".

NOTES: A. LOGICAL "1" = V_{ddq} = V_{DD150} = 1.5V. (NOMINAL)
B. NEW DELAY RULE (NDR) WILL BE BASED ON DRIVER TERMINATED OFF-CHIP.

DRIVER TRUTH TABLE

FIG. 6

INPUTS					OUTPUTS		
PAD	LT	RI	RG	VREF	Z	ZRI	COMMENTS
-	-	-	0	-	0	RI	TEST MODE
-	-	0	-	-	0	RI	TEST MODE
1[1]	0	1	1	-	1	RI	FUNCTIONAL MODE
0[2]	0	1	1	-	0	RI	FUNCTIONAL MODE
1[3]	1	1	1	-	1	RI	BYPASS MODE
0[4]	1	1	1	-	0	RI	BYPASS MODE

1. PAD INPUT REQUIRES HSTL LEVEL "HIGH" AND $V_{ddq} < V_{dd}$.
2. PAD INPUT REQUIRES HSTL LEVEL "LOW."
3. PAD INPUT REQUIRES CMOS LEVEL "HIGH" AND $V_{ddq} = V_{dd}$.
4. PAD INPUT REQUIRES CMOS LEVEL "LOW."

RECEIVER TRUTH TABLE

FIG. 7

RI	RECEIVER INHIBIT INPUT (RI IN)
PADR	EXTERNAL RESISTOR NODE 1 OF 2
PADG	EXTERNAL RESISTOR NODE 2 OF 2
ZRI	RECEIVER INHIBIT OUTPUT (RI OUT)
POR	POWER ON RESET
XFER	TRANSFER DATA TO LATCH
SENSE	NULL SENSE-AMPLIFIER
EVAL	EVALUATE IMPEDANCE
CNTN0	NFET PVT COUNT BIT 0 (LSB)
CNTN1	NFET PVT COUNT BIT 1
CNTN2	NFET PVT COUNT BIT 2
CNTN3	NFET PVT COUNT BIT 3
CNTN4	NFET PVT COUNT BIT 4
CNTN5	NFET PVT COUNT BIT 5 (MSB)
CNTP0	PFET PVT COUNT BIT 0 (LSB)
CNTP1	PFET PVT COUNT BIT 1
CNTP2	PFET PVT COUNT BIT 2
CNTP3	PFET PVT COUNT BIT 3
CNTP4	PFET PVT COUNT BIT 4
CNTP5	PFET PVT COUNT BIT 5 (MSB)
PVTP0	PFET PVT CONTROL BIT 0 (LSB)
PVTP1	PFET PVT CONTROL BIT 1
PVTP2	PFET PVT CONTROL BIT 2
PVTP3	PFET PVT CONTROL BIT 3
PVTP4	PFET PVT CONTROL BIT 4
PVTP5	PFET PVT CONTROL BIT 5 (MSB)
ZPCNTDWN	COUNT DOWN PFET FINGERS
ZNCNTDWN	COUNT DOWN NFET FINGERS

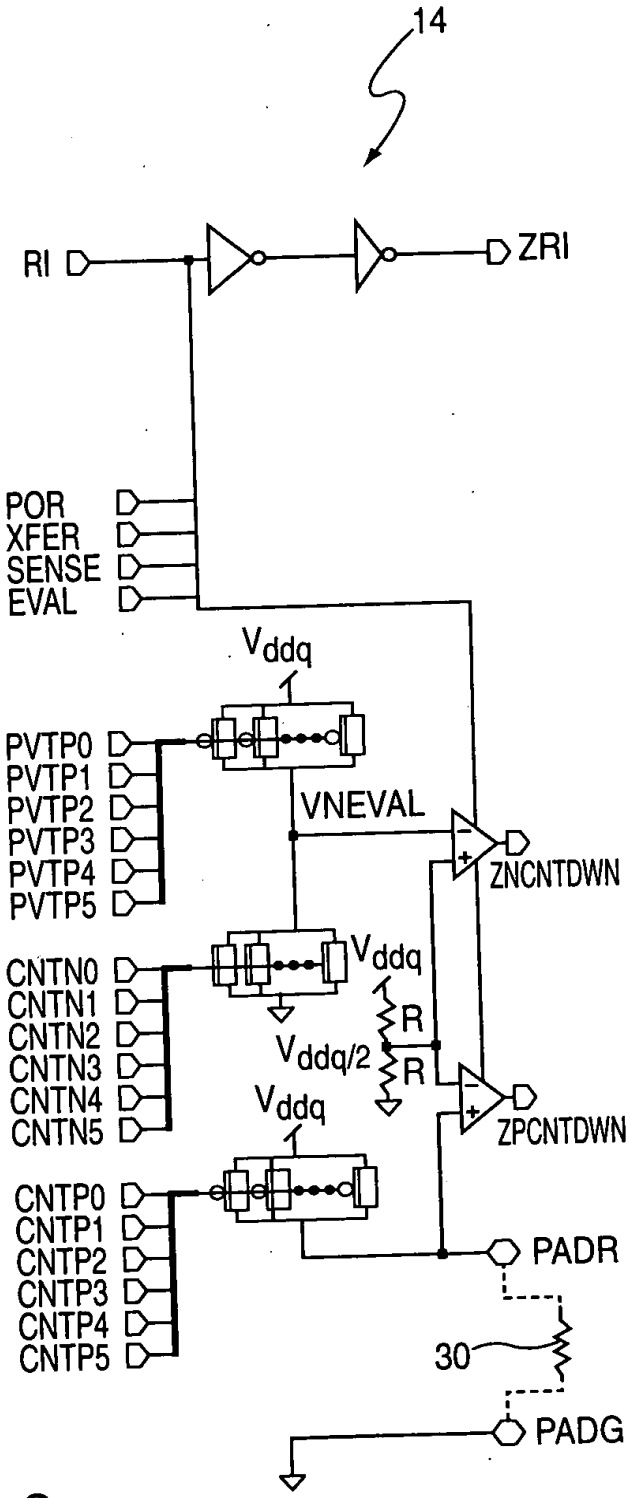


FIG. 8

INPUTS						OUTPUTS	
RI	POR	EVAL	SENSE	XFER	CNTN0-CNTN5 CNTP0-CNTP5 PVTP0-PVTP5	ZPCNT DWN	ZNCNT DWN
0	X	X	X	X	X	0	0
X	0	X	X	X	X	0	0
1	1	1	1	1	X	X[1]	X[1]
1	1	1	0	1	X	1[2]	1[3]
1	1	1	0	1	X	0[4]	0[5]
1	1	1	0	0	X	LATCH[6]	LATCH[6]
1	1	0	0	0	X	HOLD[7]	HOLD[7]

1. EVAL = 1, POWER UP THE CELL; SENSE = 1, NULLS COMPARATOR INPUTS.
2. ZPCNTDWN = 1, WHEN VPADR > $V_{ddq}/2$
3. ZNCNTDWN = 1, WHEN VNEVAL < $V_{ddq}/2$
4. ZPCNTDWN = 0, WHEN VPADR < $V_{ddq}/2$
5. ZNCNTDWN = 0, WHEN VNEVAL > $V_{ddq}/2$
6. XFER = 0, LATCHES THE COMPARATOR OUTPUTS.
7. THE REFERENCE I/O IS POWERED DOWN AND THE PRESENT STATES OF THE OUTPUTS ARE HELD.

REF TRUTH TABLE

FIG. 9

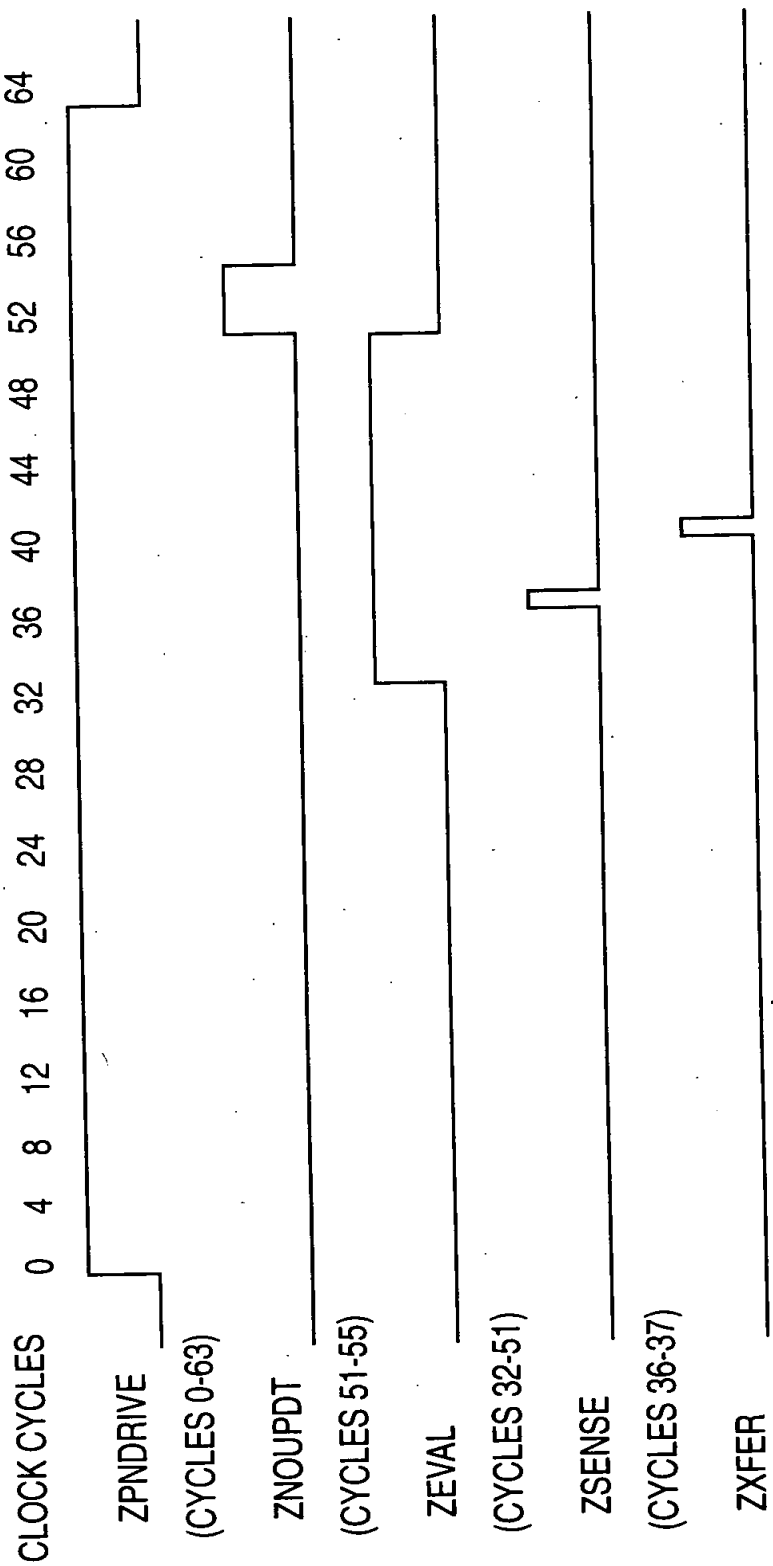

CLOCK CYCLES 0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64
ZPNDRIVE
(CYCLES 0-63)
ZNOUPDT
(CYCLES 51-55)
ZEVAL
(CYCLES 32-51)
ZSENSE
(CYCLES 36-37)
ZXFER
(CYCLES 40-41)

FIG. 10